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Design and Simulation of Circuit for Synchronization of Multidelay Feedback Systems

Abstract. *This paper presents the design of electronic circuit for multidelay feedback systems and synchronization of multidelay feedback systems. There, dynamical equation for driving signal is in the form of the sum of multiple nonlinear transformations of delayed state variable. The circuit of modified Mackey-Glass system and synchronization are demonstrated by SPICE. The simulation results proof the existence of the scheme of complete synchronization between the Master and Slave and synchronization is maintained during interaction.*

Introduction

Time delay systems can exhibit a highly complicated dynamics [1] and they bring potential applications in secure communications [2]. Circuits for single delay systems as well as for synchronous systems have been experimented and reported [3, 4]. Recently, multiple delayed systems and synchronization of coupled multidelay systems have been interested increasingly due that higher security can be achieved [5]. This paper presents a electronic circuit design for multiple delayed systems and complete synchronization of coupled multidelay feedback systems. The multidelay Mackey-Glass system is chosen as an exemplar to demonstrate for the design using SPICE.

Circuit design of multidelay feedback systems

Let's start considering a multiple delay feedback system whose dynamical equation is defined as below:

$$\frac{dx}{dt} = -\alpha x + \sum_{i=1}^{P} m_i f(x_{\tau_i}) \tag{1}$$

where α, m_i, $\tau_i \in \Re$; P is an integer. The delayed state variable x_{τ_i} stands for $x(t-\tau_i)$. Note that nonlinear function $f(.)$ is differentiable, generic. Assumed that $\alpha \neq 0$, Eq.(1) can be reduced by dividing the right hand-side terms by α and scaling the time quantities $t \to \alpha t$, $\tau \to \alpha\tau$:

$$\frac{dx}{dt} = -x + \frac{1}{\alpha}\sum_{i=1}^{P} m_i f(x_{\tau_i}) \tag{2}$$

The analog circuit design representing for the system (2) is illustrated as in Fig. 1(a). The dynamics of the circuit model can be written as

$$C_0\frac{dU}{dt} = \frac{U_{ND}(t) - U(t)}{R_0} \tag{3}$$

where $U_{ND}(t) = \sum\limits_{i=1}^{P} U_{ND_i}(t)$; $U_{ND_i}(t) = g_i f(U(t-\tau_i))$ and g_i is gain factor. Dimensionless variable x, time t and dimensionless delay τ_i are introduced as below

$$\frac{U}{U_{ss}} = x', \quad \frac{t}{R_0C_0} = t', \quad \frac{\tau_i}{R_0C_0} = \tau_i' \tag{4}$$

where U_{ss} is steady state solution of (3). Hence, (3) can be rewritten as

$$\frac{dx'}{dt'} = -x' + \lambda(x') \tag{5}$$

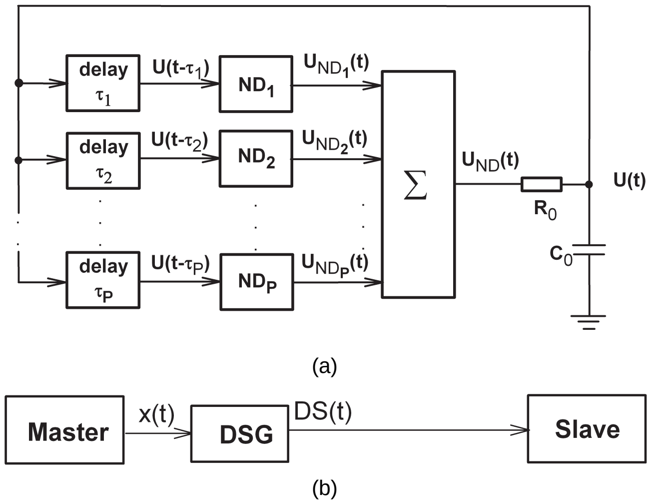

Figure 1. (a) Circuit of multidelay feedback systems, (b) Synchronization of multidelay feedback systems

where $\lambda(x') = \frac{U_{ND}(t)}{U_{ss}} (= \frac{1}{U_{ss}} \sum\limits_{i=1}^{P} g_i f(U(t-\tau_i)))$. It is easy to realize that $\lambda(x')$ is isomorphic to the second right-side term of (2).

Circuit design of synchronization of coupled multidelay feedback systems

In this section, the circuit model for complete synchronization of coupled multidelay feedback systems is presented. The dynamical equations for synchronization system are as

$$\begin{aligned} Master &: \frac{dx}{dt} = -\alpha x + \sum_{i=1}^{P} m_i f(x_{\tau_i}), \\ Drivingsignal &: DS(t) = \sum_{i=1}^{Q} k_i f(x_{\tau_{P+i}}), \\ Slave &: \frac{dy}{dt} = -\alpha y + \sum_{i=1}^{P} n_i f(y_{\tau_i}) + DS(t), \end{aligned} \tag{6}$$

where $k_j, \tau_i \in \Re$ and Q are positive integers. Note that driving signal is the sum of multiple nonlinearly transformed components of the delayed state variable, and produced by driving signal generator (DSG) as in Fig. 1(b). As described in [6], the relation between parameters for the scheme of complete synchronization is $m_i - k_j = n_i$. In addition, the condition for the existence of complete synchronization manifold of $y(t) = x(t)$ is

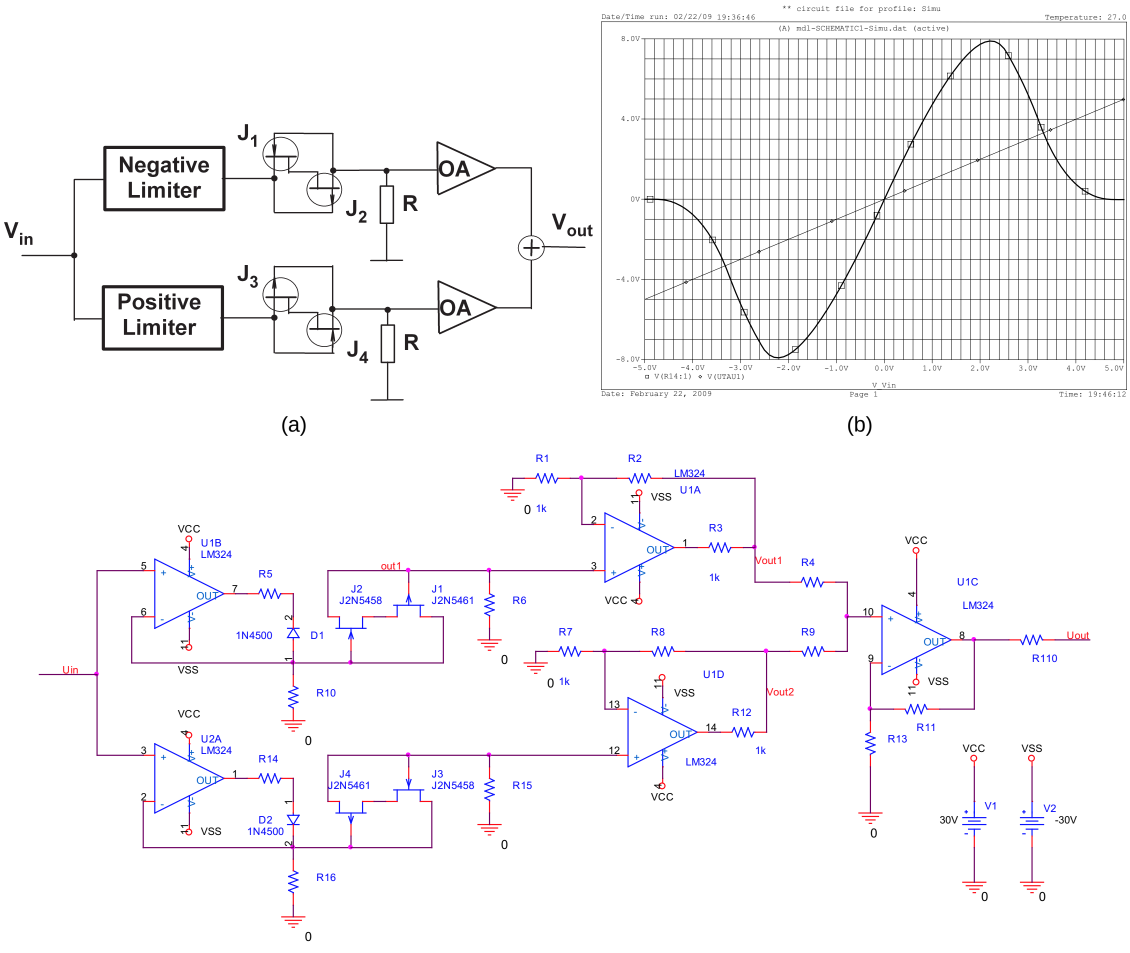

Figure 2. (a) Nonlinear model, (b) Characteristic curve, (c) Circuit schematic for nonlinear function.

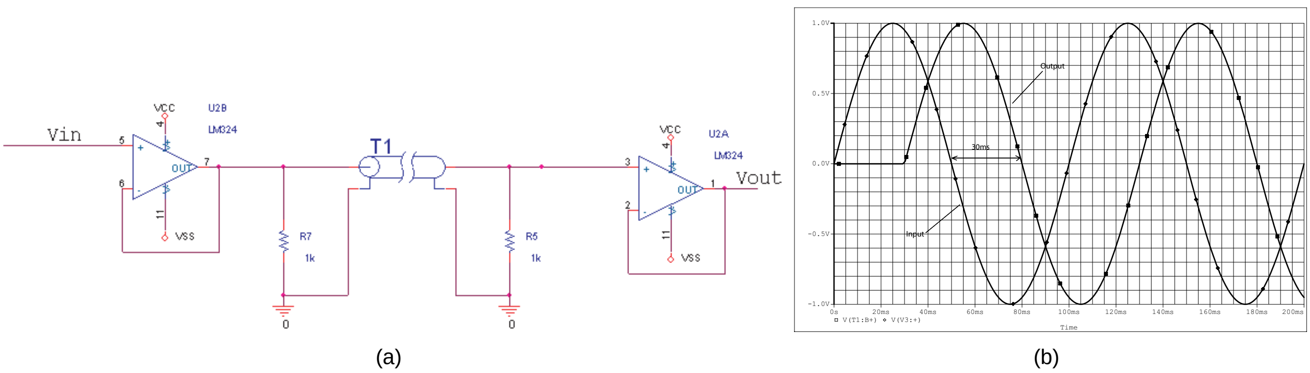

Figure 3. (a) Delay line, (b) Simulation result for delay line.

$$\alpha > \sum_{i=1}^{P} |n_i| \left| (\sup f'(x_{\tau_i})) \right|, \tag{7}$$

The assumption for the relation between delays is $\tau_{P+i} = \tau_i$ for $i = 1..P$.

Simulation

The general description is demonstrated with the circuit of two-delay Mackey-Glass systems. The dynamical equation is in the form of modified Mackey-Glass system is as below

$$\frac{dx}{dt} = -\alpha x + \sum_{i=1}^{P=2} m_i \frac{x_{\tau_i}}{1 + x_{\tau_i}^{10}} \tag{8}$$

where α is taken a nonzero, positive real value. Assume that $t \to \alpha t$ and $\tau \to \alpha\tau$, (8) can be rewriten as

$$\frac{dx}{dt} = -x + \frac{1}{\alpha} \sum_{i=1}^{P=2} m_i \frac{x_{\tau_i}}{1 + x_{\tau_i}^{10}} \tag{9}$$

The value chosen for delays and system parameters is $\alpha = 0.1$, $m_1 =$ and m_2 is as 0.1, 1.0 and 1.5, respectively. There are several ways [7, 8] to build the circuits whose transfer function exhibits as $f(x) = \frac{x}{1+x^b}$. In this example, a couple of two complementary junction field-effect transistors (JFETs) as described by Chua *et al.* [8] is used for functioning as a nonlinear device with a function of $f(x)$. Fig.2 illustrates the circuit and its transfer function. As shown in Fig.2(a), the input signal is dealt with positive and negative

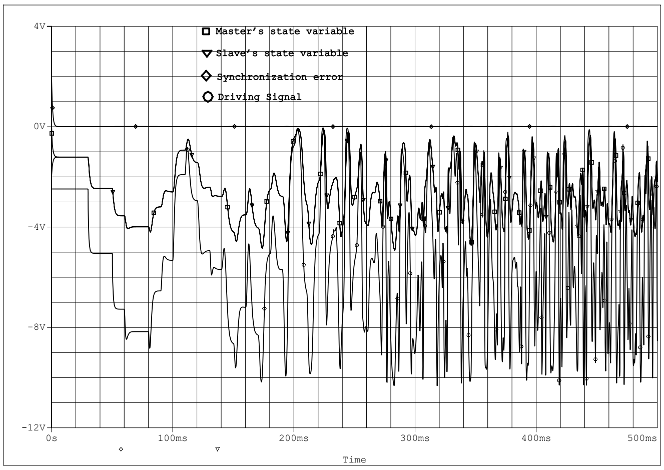

Figure 5. Simulation result for synchronization system.

parts separately, that is due to the characteristic curve of coupled JFETs. The separation is done by using limiters. This is different from the circuit realizing for Mackey-Glass's system with single delay as described in [3, 4], where the signal presenting for the state variable oscillates in the range greater that zero. The characteristic curve as presented in Fig.2(b) is obtained by simulating the circuit in Fig.2(c), there, the limiters are built by ideal diodes. It is easy to observe the characteristic curve from Fig.2(b) that the nonlinear circuit as given in Fig.2(a) can operate with a bipolar input signal. The gain factor of the circuit represents for $\frac{m_i}{\alpha}$ and can be adjusted via the value of resistors R_1, R_2, R_7 and R_8.

A lossless transmission line is used as a delay line in the design and simulation. The schematic for the delay line is displayed in Fig.3(a). The simulation result for delay of 30ms is shown in Fig.3(b); there the input signal is sine wave. In practical, the state variable is delayed by using either a series of LC or integrated bucket brigade delay line (National Panasonic, MN3011).

The schematic for simulation for synchronous system of multiple delay system with the equations described in (9) is depicted in Fig.4, where the driving signal is in the form of two delays. The adopted values of resistors are to obtain the scheme of complete synchronization as shown in the schematic. It is emphasized that the value chosen for integrator is the capacitor of $C_0 = 0.1uF$ and the resistor of $R_0 = 100K$. The value for two delays is chosen for the Master, Slave and DSG with $\tau_1 = 0.03s$ and $\tau_2 = 0.05s$, in other words, complete synchronization scheme exhibits. In the simulation, the initial condition chosen for the capacitors, C_1 at the Master and C_2 at the Slave is 0.02 volts and 2.0 volts, respectively. It is easy to observe from the simulation result displayed in Fig.5 that the Slave's and Master's state variables are keeping up each other. Moreover, it is clear that the synchronization error $e(t) = y(t) - x(t)$ vanishes eventually.

Conclusions

This paper presents the design and simulation of circuit for multiple delay systems and for synchronization of multiple delay systems. The simulation results proof the effectiveness of electronic designs and the existence of complete synchronization manifold in the synchronous circuit as prediction.

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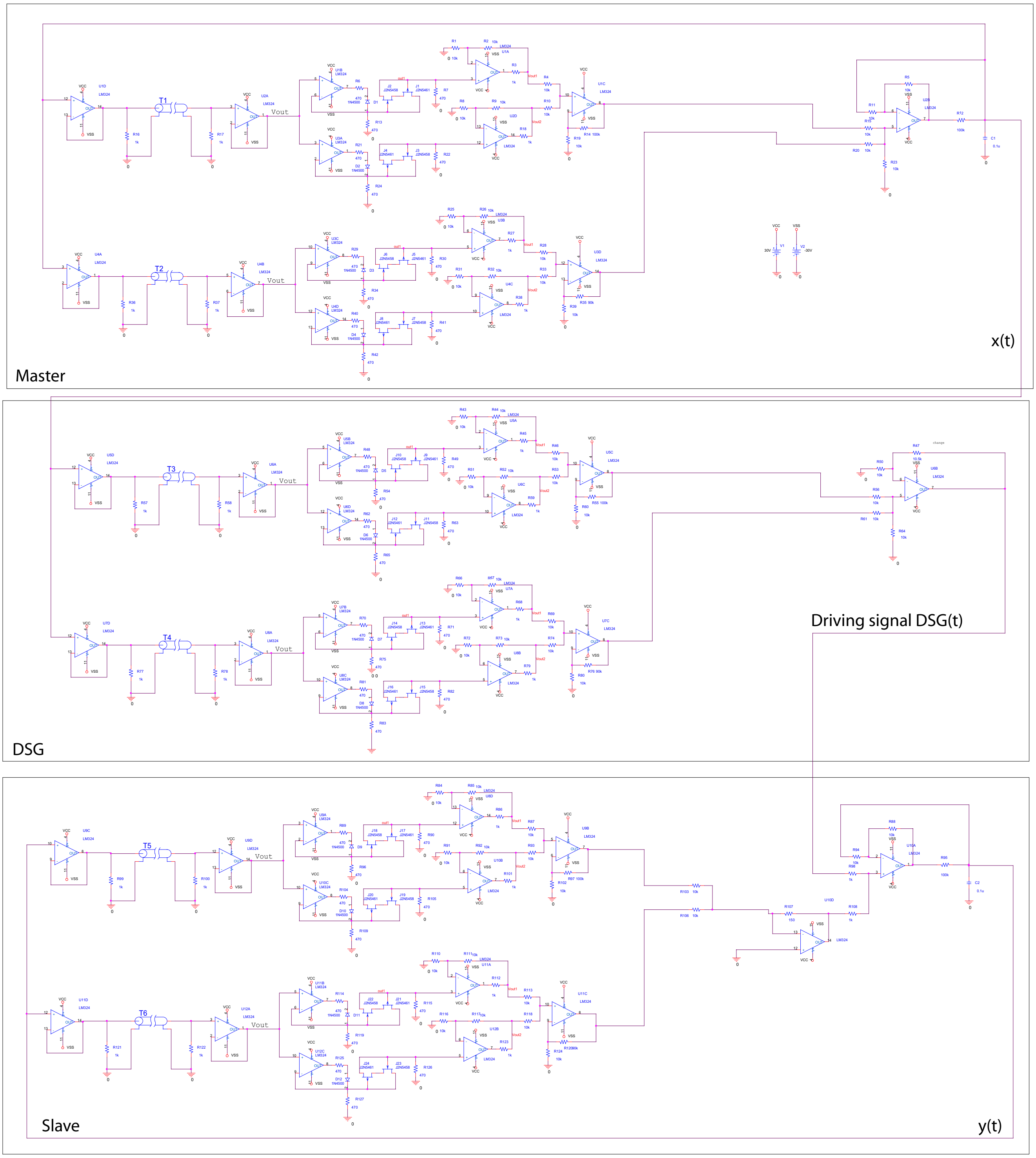

Figure 4. Schematic of synchronization system.